ANALYSIS OF R-2R DIGITAL-TO-ANALOG CONVERTER WITH EQUAL CURRENT SWITCHING

BY

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THESIS

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ABSTRACT

Analysis and performance tradeoffs of an R-2R digital-to-analog converter with equal current switching are presented. It is shown that for such architecture, the active area of the DAC grows as the resolution increases due to higher matching requirement needed. A fully binary-weighted DAC suffers from well-known differential linearity problems and large switching glitches at the output, while a fully thermometer-coded DAC benefits from the relaxed DNL but requires a large area to realize. The R-2R DAC with equal current switching into the ladder network can be implemented using very low currents with more relaxed current matching requirements over the binary-weighted DAC, and less area over the thermometer-coded DAC.

To my parents, for their love and support.

ACKNOWLEDGMENTS

I would like to express my sincere gratitude to my academic adviser, Dr. Chandrasekhar Radhakrishnan, who constantly encourages and motivates me throughout my graduate studies. I am thankful to him for providing me with the best opportunities. He has been a great mentor. I also thank Professor Pavan Kumar Hanumolu, my research adviser, under whose guidance the work in the thesis was developed.

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ADC	Analog-to-digital converter
DAC	Digital-to-analog converter
DNL	Differential non-linearity
FFT	Fast-Fourier transform
INL	Integral non-linearity
LSB	Least significant bit
MSB	Most significant bit
MOSFET	Metal oxide silicon field-effect transistor
OpAmp	Operational amplifier
Std	Standard deviation
SFDR	Furious-free dynamic range
SNR	Signal-to-noise ratio
VCCS	Voltage controlled current source

CHAPTER 1

INTRODUCTION

Digital-to-analog converters (DACs) form the basis of any signal processing system that interacts with the real world. A DAC acts as the interface between the digital and analog worlds as it transforms digital code into an analog signal. DACs with high speed, precision and low power dissipation are in high demand for many applications such as communications, audios and controls. Numerous types of DACs, such as binary-weighted, thermometer-coded, etc., have been designed to meet the specifications. However, they have their advantages and drawbacks in achieving high performance.

1.1 Motivation

A conventional R-2R DAC can be realized in voltage or current mode. The current mode R-2R DAC requires a final operational amplifier (OpAmp) as current-to-voltage converter and complementary input signal. The final OpAmp needs to be carefully designed to obtain good stability, high gain and low offset in order to achieve high linearity. The OpAmp requirements become more complicated for higher precision converters. Similarly, the voltage mode R-2R DAC also requires a final OpAmp and shares the same stringent OpAmp requirement as the current mode R-2R DAC. Both architectures require $2N$ switches (usually implemented using MOSFETs) in the R-2R DAC ladder, and the on-resistance of the MOSFETs, R_{ON}, varies depending on the digital code. The mismatches among R_{ON} in the switch MOSFETs contribute to DAC nonlinearity and degrade the performance of the converter [1].

The goal of this thesis is to implement equal current sources switched into R-2R ladder network which eliminate the need for the final OpAmp and the effect of switches in the ladder network. The proposed architecture uses

unit element current steering which operates in binary without needing of a decoder to convert the binary code to thermometer code. It incorporates the advantages from binary-weighted DAC as well as from the thermometer coded DAC without performing segmentation. The design was done in the Cadence Virtuoso Environment using a 65 nm process and the results were verified in simulation.

1.2 Outline

This thesis is organized as follows: Chapter 2 provides an introduction to digital-to-analog converters (DACs), their basic architectures and performance metrics. Chapter 3 provides the design overview of a conventional R-2R DAC followed by the proposed R-2R DAC and its challenges in achieving high performance. This chapter also includes the behavioral mode and transistor level prototyping on the proposed DAC. Chapter 4 reports the simulation result of the proposed DAC in behavior mode and transistor level. An analysis of the simulation results is also provided in this chapter. Finally, we conclude the thesis in Chapter 5.

CHAPTER 2

DATA CONVERTERS OVERVIEW

A digital-to-analog converter (DAC) produces an analog output V_A that is proportional to the digital input D. The digital input is normally represented in binary. Each digital code represents a corresponding output voltage while these voltages create a pulse amplitude signal that has a staircase-like pattern [2]. The difference between binary and thermometer code for a 3-bit DAC can be seen in Table 2.1. The resolution of a DAC is determined by the number of binary input bits. A DAC with N-bit resolution produces 2^N output voltages. Most DAC architectures work by having a constant reference voltage V_{ref}. The reference voltage is divided into smaller references that correspond to the digital input.

Table 2.1: Binary vs. thermometer code

Decimal, D	Binary	Thermometer
0	000	0000000
1	001	0000001
2	010	0000011
3	011	0000111
4	100	0001111
5	101	0011111
6	110	0111111
7	111	1111111

The analog output V_A at any given digital input can be determined by (2.1). The minimum step size in the analog output of a converter is often known as one LSB and is defined in (2.2). For a 3-bit DAC, the smallest possible output change at the LSB input will change the output voltage by $\frac{1}{2^3}$ or 12.5% of the reference voltage. Since the digital code of 0 corresponds to the minimum analog output voltage, the maximum analog output voltage will be one LSB less than V_{ref} and the converter is said to have a full-scale range from minimum output voltage to the maximum output voltage. The

full-scale voltage V_{FS} can be expressed as (2.3). Table 2.2 shows an example of the input and output of a 3-bit DAC.

$$V_A = V_{ref}(\frac{D}{2^N}) \tag{2.1}$$

$$LSB = \frac{V_{ref}}{2^N} \tag{2.2}$$

$$V_{FS} = V_{ref}(\frac{2^N - 1}{2^N}) \tag{2.3}$$

Table 2.2: Input and output of a 3-bit DAC

Binary code	V_A
000	0
001	$1/V_{ref}$
010	$2/V_{ref}$
011	$3/V_{ref}$
100	$4/V_{ref}$
101	$5/V_{ref}$
110	$6/V_{ref}$
111	$7/V_{ref}$

2.1 Performance Metrics

A circuit implementation of a converter will suffer from various non-idealities such as component matching, noise, etc. This causes the output to become distorted and noise to be added to the signal [3]. The performance of the converter can be expressed in terms of its static and dynamic performances. The accuracy of the converter is determined by how closely the output matches the expected output at a given code. The static performance is analyzed by sweeping the full range of binary codes and observing the characteristic staircase output plot, while the dynamic performance is measured by supplying a digital sinusoidal input and analyzing the fast-Fourier transform (FFT) of the reconstructed output. The following subsections will describe the standard measures to characterize DAC and its performance.

2.1.1 Static performances

The most common static performance measures include gain and offset error, differential nonlinearity (DNL) and integral nonlinearity (INL). In general, offset error usually does not impact the performance of the converter because all output codes are uniformly affected by the offset. A linear gain error also does not affect the converter but a non-linear gain will cause distortion. The gain and offset error should be compensated (or removed) before measuring the DNL and INL.

Gain and offset error

An offset error is defined as the difference between the ideal and actual analog outputs that correspond to an input code of all zeros, while a gain error is the deviation of the slope of the line passing through the end points from its ideal value.

Differential nonlinearity (DNL)

DNL is the deviation in the output step size from the ideal value of one least significant bit (LSB) [2]. As an example, if the step between two adjacent codes is 1.4 LSB, then the DNL at that code transition is said to be 0.4 LSB. In order to maintain good accuracy, the DNL must lie between $\pm 1/2$ LSB. An output transfer curve with DNL ≥ -1 LSB will result in missing code. The DNL at each code can be computed as (2.4). Unlike ADC DNL, DNL of a DAC can be less than -1 LSB.

$$DNL[m] = \frac{V[m] - V[m-1] - V[LSB]}{V[LSB]} \tag{2.4}$$

Integral nonlinearity (INL)

INL is defined as the maximum deviation of the input/output characteristic from a straight line passing through its end points. The difference between the ideal and actual characteristics will be called the INL profile [2]. The INL can be measured by sweeping the digital input and plotting the analog output. A line is then drawn from zero to the end points, and the output

deviation from this line at every code is the INL [2]. INL can also be calculated by (2.5) or by computing the cumulative sum of DNL as shown in (2.6).

$$INL[m] = \frac{V[m] - V[idea]}{V[LSB]} \tag{2.5}$$

$$INL[m] = \sum_{i=1}^{m-1} DNL[i] \tag{2.6}$$

Monotonicity is guaranteed if $|INL| \leq 0.5$ LSB which implies that $|DNL| \leq 1$ LSB. A profile of large INL and small DNL implies that there is smooth variation in the transfer curve, while a profile with large DNL and small INL means that there is abrupt variation in the transfer curve.

2.1.2 Dynamic performances

In the previous subsection, the DAC is regarded as a discrete-time circuit; the analog output levels are valid at discrete time instants, i.e., the static values. In real application, the DAC is used as a continuous-time circuit, meaning the inputs fed into the DAC are constantly changing. Due to switching of analog elements in the DAC circuit, the outputs are signal-dependent and hence exhibit dynamic behavior. The most common dynamic performances are finite settling time, glitches, signal-to-noise ratio (SNR), and spurious-free dynamic range (SFDR)

Finite settling time and glitches

The settling time is the time required for the output to experience full-scale transition and settle within an absolute percentage of its final value [2]. The settling time is dependent on the RC time constants. A glitch occurs when the switching time instants of different bits in a DAC are unmatched. For a short time, false code could appear at the output due to a glitch. For a binary-weighted DAC, a large glitch will appear during midcode transition ($0111\cdots111$ to $1000\cdots000$) when the MSB is switching faster than the LSBs ($1111\cdots111$).

Signal-to-noise ratio (SNR)

The SNR is defined as the ratio of the signal power to the total noise at the output when a digital sinusoidal input is fed into the converter. In the ideal DAC, the noise power consists of the quantization noise, but in a practical converter, errors from linearity, glitches, output settling time, etc., will increase the total noise power, degrading the SNR. The SNR of the R-2R DAC will be derived in Section 3.3. An ideal SNR for an N-bit converter can be expressed as (2.7)

$$SNR = 6.02N + 1.76 \text{ dB} \tag{2.7}$$

Spurious-free dynamic range (SFDR)

Another important specifications for DAC is the spurious-free dynamic range (SFDR). The SFDR of a signal is the ratio of the power due to its input signal to the power of the largest distortion component (also known as a spur) in the spectrum. The SFDR of a signal is given by (2.8).

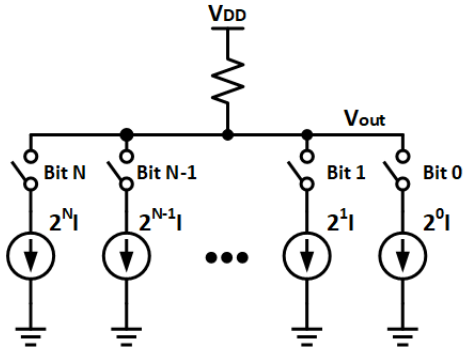
$$SFDR = 10\, log_{10}(\frac{P_{signal}}{P_{spur}}) \tag{2.8}$$

2.2 DAC Architectures

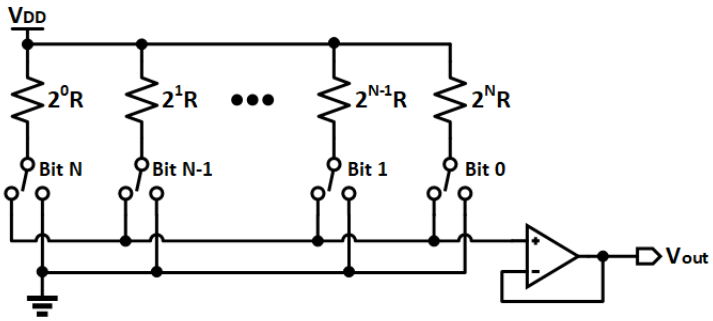
There are many different ways to implement DAC and the choice depends on the application of the converter. Area, power, bandwidth, accuracy, etc., are the factors that could affect the choice of the DAC architecture. Some DAC architectures are very simple. They consist of only switches and resistors, but are limited in resolution and speed, and suffer from strict device matching [4]. These architectures can be improved by applying different coding schemes, such as thermometer encoding instead of binary. There are two main DAC architectures, namely binary-weighted and thermometer-coded DAC. The combination of binary-weighted and thermometer-coded DAC is known as hybrid segmented DAC.

2.2.1 Binary-weighted architecture

There are two ways to implement a binary-weighted DAC: current sources and resistors. Fig. 2.1a shows a conceptual circuit of an N-bit binary-weighted DAC using current steering and Fig. 2.1b shows another example of binary-weighted DAC using resistor ladder. Whether implemented using current sources or resistors, each component carries binary-weighted values.



(a) Current steering DAC



(b) Resistor ladder

Figure 2.1: Binary-weighted DAC architecture

(a) Current steering

The current steering DAC works by summing the current produced by an array of current sources. One end of a load resistor is connected to the summing node of the current sources, and the other end is connected to the supply voltage [5]. When the current source is enabled, the summing current flows through the resistor and causes voltage drop across the resistor, thereby converting the current into output voltage. Since this architecture does not require an OpAmp as current-to-voltage converter, the circuit implementation is simpler. A binary-weighted current

steering DAC can easily be implemented using only N current sources and switches, where N is the of the converter [5].

(b) Resistor ladder

The binary-weighted resistor DAC shown in Fig. 2.1b is built using a resistor network consisting of N resistors. The MSB resistor has a resistance of R and the resistance will double for each descending bit. Each resistor is connected to a switch that is controlled by the binary input and the other end of the switch is connected to an OpAmp. The Opamp is used as current-to-voltage converter: a reference voltage connected to the resistor ladder allows current to flow through the resistor to the virtual ground of the OpAmp, forming the output [5].

The binary weighted DAC is simple to implement as no decoding scheme is required [6]. However, there are several major drawbacks to such a DAC. A large glitch can occur at the output during certain switching code. For example, for current steering DAC, at the midcode transition ($011 \rightarrow 100$), the most significant bit (MSB) current source is turned on while all the other current sources will be turning off. If the MSB current source fails to reach its final value before the other sources switch off, then a glitch will occur. In addition, the MSB current source needs to be matched to the sum of the other current sources to within 0.5 LSBs to achieve good accuracy [5]. The MSB resistor in resistor ladder DAC also needs to be precisely matched with other resistors. For a 10-bit binary-weighted DAC, the MSB current source requires $2^{10}I$ while the LSB current source requires only I. In a resistor ladder DAC, the MSB resistor requires R while the LSB resistor requires $2^{10}R$. Due to process variation and random mismatch, matching the MSB and LSB components is very challenging, especially in higher resolution design. There are always challenges in device matching for all bit transitions, but the severity of the problem is proportional to the weight of the bit [7]. The monotonicity of the converter is not guaranteed for binary-weighted DAC. A method to reduce glitches and relax the matching requirement is to use a unary weighted array, commonly known as thermometer-coded architecture.

2.2.2 Thermometer-coded architecture

A thermometer-coded DAC contains $(2^N - 1)$ equal resistor or current sources. For example, a 3-bit current steering DAC would have 7 current sources as shown in Fig 2.2. Each unit element is controlled by the inputs coming from the binary-to-thermometer decoder [7]. When the digital input has 1 LSB of increment, one more current source is turned on and it is added to the summing current node. This architecture guarantees monotonicity as the analog output voltage always increases with the increase of digital input. There are other advantages for such architecture compared to binary-weighted DAC apart from guaranteed monotonicity. The glitch problem is also more suppressed in such architecture. Since every LSB requires a unit element, switch and decoding circuit, the major drawback of the thermometer-coded DAC is area. For example, a 10-bit DAC requires 1023 unit elements as compared to a binary-weighted 10-bit DAC which only requires 10 elements. As the converter resolution increases, the area of the binary-to-thermometer decoder also increases rapidly. Let A_{decode} be the required area for the digital decoding scheme per unit element, then the total digital area for a N-bit DAC equals to $2^N \times A_{decoder}$ [7]. To leverage the advantages of the thermometer-coded DAC with smaller area, hybrid segmented architecture can be used.

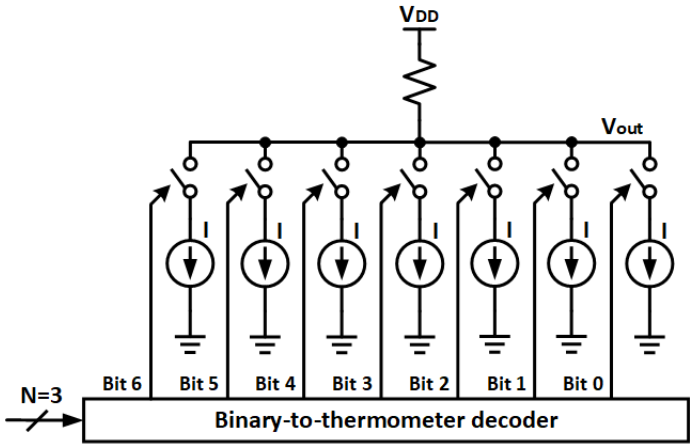


Figure 2.2: 3-bit thermometer-coded DAC architecture

2.2.3 Hybrid segmented architecture

The DAC is divided into two sub-DACs: one for the MSBs and one for the LSBs [7]. The MSB portion is implemented using thermometer-coded architecture while the LSB portion is implemented using binary-weighted architecture. Thermometer coding is used for the MSB portion because the accuracy is needed most. The area is smaller for this portion because of the reduced number of bits as compared to a purely thermometer-coded design. The LSB portion can be implemented using either binary-weighted or thermometer-coded design. If all the bits are done using the binary-weighted approach, the DAC is considered a fully binary-weighted design with 0% segmentation, whereas a fully thermometer-coded design is referred to as 100% segmented. Study has shown that the optimal segmentation can be determined from Fig. 2.3 [7]. As shown in Fig. 2.3, the required total area is first dominated by the DNL requirement as the percentage of segmentation increases, followed by the INL requirements, and finally by the decoding scheme. The flat part of the curve is the optimal percentage of segmentation for minimal area, and the total area would be determined by the INL requirement. To optimize area and obtain the best INL, the percentage of segmentation should be close to 70 [5].

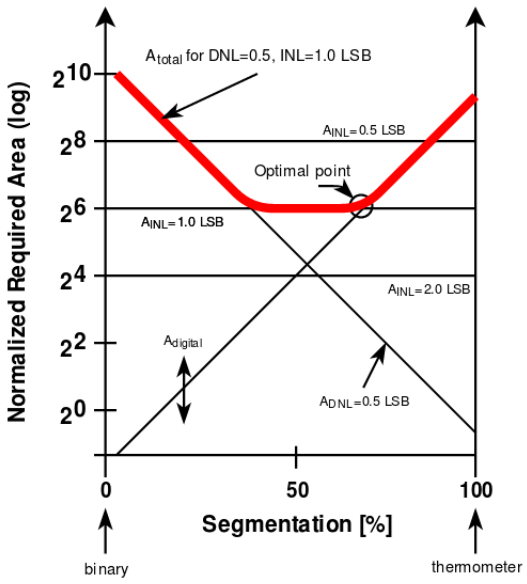


Figure 2.3: Normalized required area versus percentage of segmentation [7]

CHAPTER 3

DESIGN OF R-2R DAC

3.1 Design Overview

The conventional R-2R DAC can be implemented in current or voltage mode. For example, a R-2R DAC behaves like a binary weighted voltage divider. It consists of a 2R leg in parallel with each R resistor in series to create binary weighting. A 3-bit R-2R in Fig. 3.1 is used to explain the working mechanism of the DAC. The switch is connected either to ground or to the reference voltage, V_{ref}. When the MSB switch is connected to V_{ref} while the rest are connected to ground, the circuit can be simplified into the circuit shown in Fig. 3.2a. All voltage sources other than V_1 are shorted to ground. The equivalent resistance looking back into the ladder network from any node in the ladder is 2R. Hence, the output voltage V_{out} can be expressed as $\frac{V_1}{2}$. When the (MSB-1) bit is HIGH, the contribution from V_2 results in the Thevenin equivalent circuit shown in Fig. 3.2b, which is a voltage source of $\frac{V_2}{2}$ and a resistor R. The output voltage can thus be expressed as $\frac{V_2}{2^2}$. Finally, the contribution from the LSB simplified the output voltage to $\frac{V_3}{2^3}$ (Fig. 3.2c). By superposition, the output voltage can be expressed as:

$$V_{out} = (D_2)V_1 + (D_1)V_2 + (D_0)V_3 \tag{3.1}$$

where $D_2D_1D_0$ is the 3-bit digital code in binary with D_2 being the MSB. In general, an N-bit R-2R ladder DAC can be expressed as:

$$V_{out} = V_{ref}[D_{(N-1)}\frac{1}{2^1} + D_{(N-2)}\frac{1}{2^2} \cdots + D_0\frac{1}{2^N}] \tag{3.2}$$

A current mode N-bit R-2R ladder DAC has the same working principle as voltage mode but requires OpAmp to perform current-to-voltage conversion.

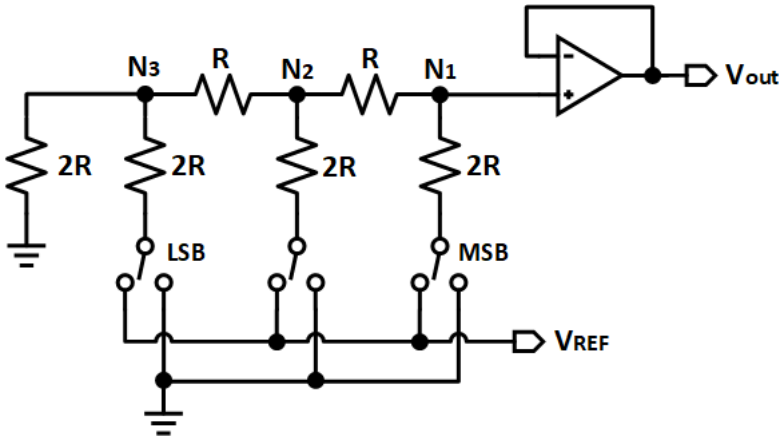
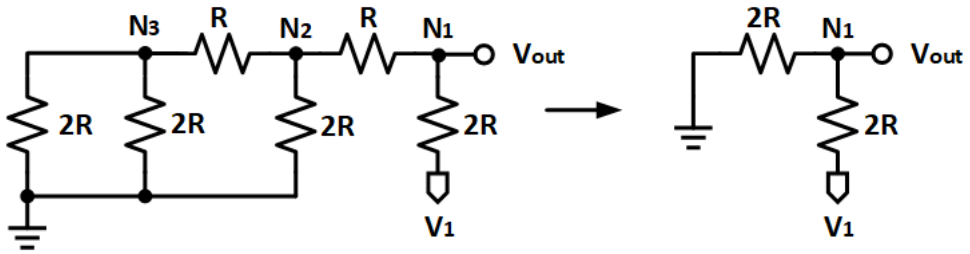
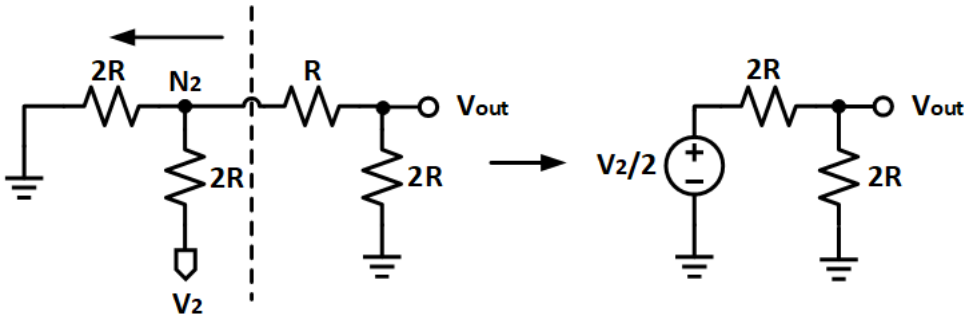


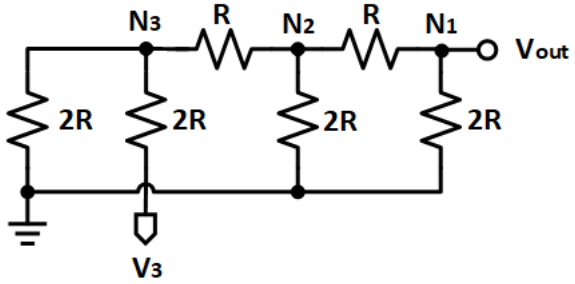
Figure 3.1: 3-bits R-2R DAC



(a) MSB = HIGH



(b) MSB-1 = HIGH



(c) LSB = HIGH

Figure 3.2: Working mechanism of 3-bit R-2R DAC [1]

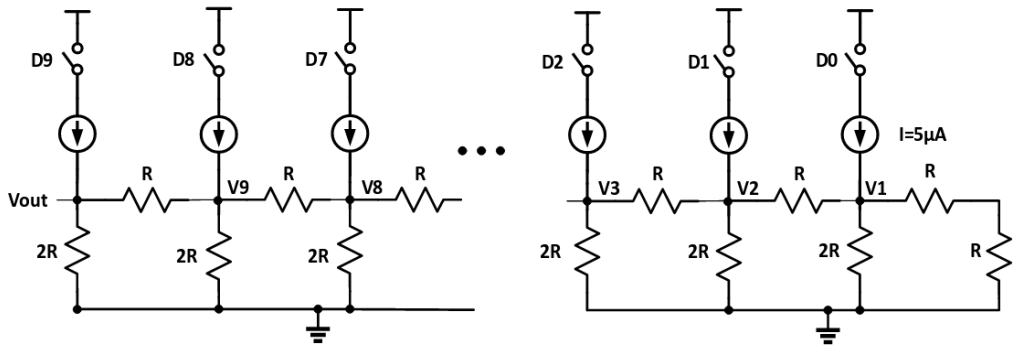
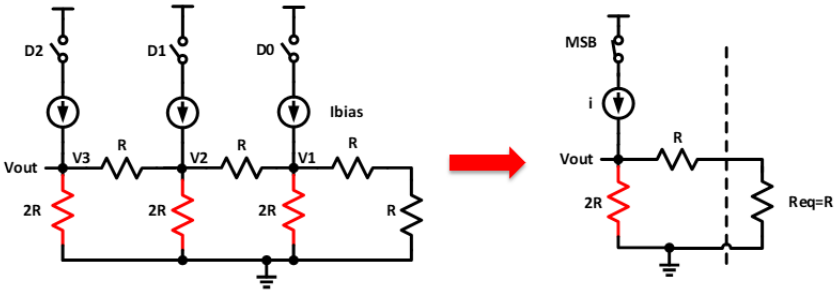
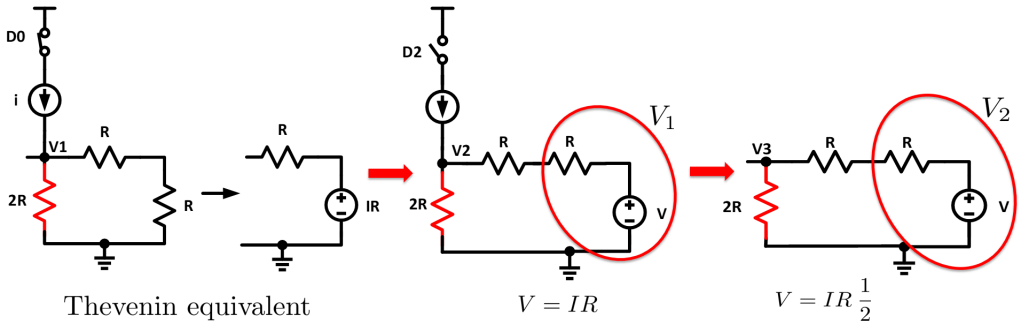


Figure 3.3: R-2R DAC with equal current switching



(a) MSB = HIGH



(b) LSB = HIGH

Figure 3.4: Working mechanism of 3-bit proposed R-2R DAC

An R-2R ladder architecture with equal current switching into the network is shown in Fig. 3.3. The working principle of the proposed architecture is again similar to conventional R-2R ladder except the reference voltage V_{ref} is determined by the biasing current and equivalent resistance R. The output swing of the DAC can be scaled to desired value by just altering the current

or resistor value. Taking 3-bit R-2R DAC as example, when the MSB is HIGH (while the rest of the bits remains low), the circuit can be simplified into Fig. 3.4a. The output voltage V_{out} is equal to $I \times R$. When the LSB is HIGH, the circuit can be transformed into the circuit shown in Fig. 3.4b with node V_1 represented by the Thevenin equivalent with $V_{thevenin} = IR$ and $R_{thevenin} = R$. This Thevenin equivalent circuit is connected to the next segment of the circuit to give $V_{thevenin} = \frac{IR}{2}$ and $R_{thevnin} = R$. This analysis method is continued until one reaches the output voltage. The output voltage when LSB is HIGH can then expressed as $V_{out} = I \times R \times \frac{1}{2^2}$.

Using superposition and the working analysis described previously, the output voltage of the proposed 10-bit R-2R DAC can be expressed as (3.3).

$$V_{out} = I \times R \times (D_9 + D_8\frac{1}{2^1} + D_7\frac{1}{2^2} + \cdots + D_1\frac{1}{2^8} + D_0\frac{1}{2^9}) \tag{3.3}$$

3.2 Source of Errors in Non-linearity

All non-ideal converters suffer from non-linearity due to component matching. Similar to the conventional R-2R ladder DAC, the R-2R DAC with equal current switching also suffers from mismatches in resistor and current branches. The types of errors introduced from the mismatches can be categorized as two main errors: systematic and random error.

3.2.1 Systematic error

Due to the fact that the DAC uses unit element current source, the matching between current sources is crucial in determining the linearity of the converter. In CMOS technology, the current sources are implemented using MOSFET. They are nominally identical and have square-law I-V characteristic [2]:

$$I_D = \frac{1}{2}\,\mu C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \tag{3.4}$$

where μ is the carrier mobility and C_{ox} is the gate oxide capacitance per unit area, W and L are the effective width and length of the device, λ is the channel length modulation, V_{DS} is the drain source voltage, V_{GS} is the gate-source voltage and V_{TH} is the threshold voltage of the MOSFET. Considering

two MOSFETs M_1 and M_2 (assuming their μ, C_{ox} and λ are the same) the systematic mismatch between M_1 and M_2 can be expressed as:

$$I_{D1} = \frac{1}{2}\mu C_{ox}\frac{W_1}{L_1}(V_{GS1} - V_{TH1})^2(1 + \lambda V_{DS1}) \tag{3.5}$$

$$I_{D2} = \frac{1}{2}\mu C_{ox}\frac{W_2}{L_2}(V_{GS2} - V_{TH2})^2(1 + \lambda V_{DS2}) \tag{3.6}$$

$$\frac{I_{D1}}{I_{D2}} = \frac{\frac{W_1}{L_1}(V_{GS1} - V_{TH1})^2(1 + \lambda V_{DS1})}{\frac{W_2}{L_2}(V_{GS2} - V_{TH2})^2(1 + \lambda V_{DS2})} \tag{3.7}$$

Assuming the gate-sources voltage of M_1 and M_2 are the same, the current sources suffer from systematic mismatch due to $V_{DS1} \neq V_{DS2}$. This error is important because the node voltages vary from each other during switching. The node voltages are the V_{DS} of the MOSFETs. Hence, the current sources differ from each other at any digital code. The variance of the systematic error is defined as (3.8)

$$\sigma^2_{\Delta I_D/I_D} \approx \lambda \Delta V_{DS} \tag{3.8}$$

3.2.2 Random error

Random error exists in both resistors and current sources. In an ideal case, the value of a resistor can be expressed as

$$R = \frac{\rho L}{Wt} = R_s\frac{L}{W} \tag{3.9}$$

where ρ is the resistivity, R_s is the sheet resistance with the unit of Ω/sq, and L, W and t are the length, width and thickness of resistors. Due to sheet resistance and dimensional variation, the resistor suffers from random mismatch. The overall mismatch between two resistors can be expressed as:

$$\frac{\Delta R}{R} = \frac{\Delta R_s}{R_s} + \frac{\Delta L}{L} - \frac{\Delta W}{W} \tag{3.10}$$

In a typical process, R_s is given, leaving L, W and R as design control. In MOSFET current sources, assuming the devices sizes W and L are equal, the current mismatch between two current sources can be found by taking

the total differential of (3.4) and dividing the result by I_D:

$$\frac{\Delta I_D}{I_D} = \frac{\Delta\beta}{\beta} - \frac{2\Delta V_{TH}}{V_{GS} - V_{TH}} \tag{3.11}$$

$$\sigma^2_{\Delta I_D/I_D} = \sigma^2_{\Delta\beta/\beta} + \frac{4\sigma^2_{\Delta_{VT}}}{(V_{GS} - V_{TH})^2} \tag{3.12}$$

where $\sigma_{\Delta V_{TH}} = \frac{A_{VT}}{\sqrt{WL}}$ [mV/μm] and $\sigma_{\Delta\beta/\beta} = \frac{A_\beta}{\sqrt{WL}}$ [%/μm]. From (3.12), the current mismatch due to random error is mainly affected by the overdrive voltage, $V_{OV} = V_{GS} - V_{TH}$ and the size of the device. In order to minimize the current mismatch, large overdrive voltage and sizing of the transistor are needed.

3.3 Noise Analysis

The signal-to-noise ratio (SNR) of the R-2R DAC is greatly dependent on the resistor and MOSFET thermal noise. Since all the current cells in the R-2R network have the same size and operating current, the total thermal noise at the output, i^2, can be expressed as (3.13), where i_n^2 is the MOSFET channel thermal noise of each current cell, $\frac{4KT}{R}$ is the thermal noise of the resistor ladder, and R is the equivalent resistor of the R-2R ladder. The channel thermal noise, i_n^2, is given by (3.14), where γ is estimated to be 2/3 and g_m is the transconductance of the current cell.

$$i^2 = \frac{4KT}{R} + \sum_{i=0}^{N} \frac{i_n^2}{4^i} \tag{3.13}$$

$$i_n^2 = 4KT\gamma g_m \tag{3.14}$$

Assuming a sinewave with peak-to-peak voltage equal to $2 \times IR$ is given as the input of the DAC, the SNR of an N-bit R-2R DAC can be written as (3.15).

$$SNR = \frac{(\frac{2\times IR}{2\sqrt{2}})^2}{\frac{4KT}{R} + \sum_{i=0}^{N} \frac{i_n^2}{4^i}} \tag{3.15}$$

The equation above is derived neglecting the quantization error.

3.4 Behavior Mode Prototype

Before getting into the transistor level design, the proposed architecture is modeled using ideal current sources and resistor. The following description is based on the design specification in Table 3.1 for a 10-bit DAC. The current sources are modeled using voltage controlled current source (VCCS) as shown in Fig. 3.5 with NC+ connected to the digital code. Whenever the digital code is HIGH, the VCCS will allow current to flow into the R-2R network branches.

Table 3.1: Parameter and specification for 10-bit R-2R DAC

Parameter	Specification	Unit
Vout	0-200	mV
Current	5	μA
Resistor	20	kΩ

Fig. 3.6a shows the high-level schematic view of the ideal R-2R network DAC with each R-2R_UA implemented as the circuit shown in Fig. 3.6b.

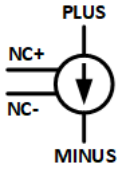
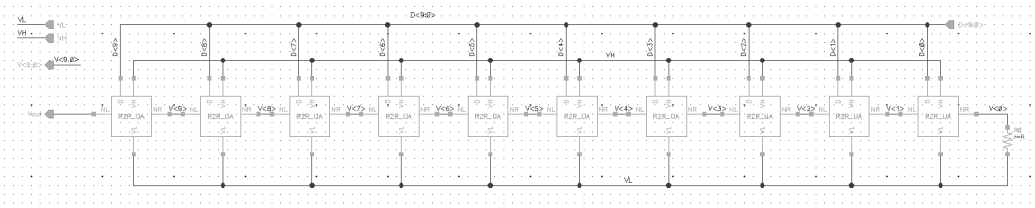
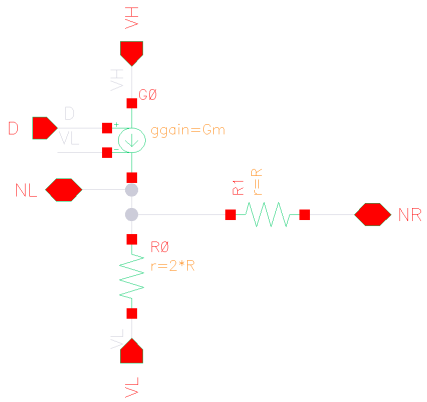


Figure 3.5: Model of voltage controlled current source



(a) 10-bit R-2R network DAC



(b) R-2R_UA

Figure 3.6: Behavioral modeling of R-2R network DAC

3.5 Transistor Level Prototype

After verifying the expected output using the behavioral modeling, the transistor level prototype is carried out to further illustrate the validity of this approach. The transistor level prototype consists of several blocks which are described in the following subsections.

3.5.1 Voltage biasing

In order to produce current sources, current biasing is needed to provide constant voltage biasing. The design of voltage biasing defines the behavior of the current source. As shown in Fig. 3.7, M_{P22} is responsible for providing the voltage biasing for the cascode PMOS while the gate voltage of M_{P1} provides the voltage biasing for M_1 of the current source.

The size of the MOSFETs in Fig. 3.7 is determined by first choosing the desired overdrive voltage. The size of M_{P1} is determined by the chosen

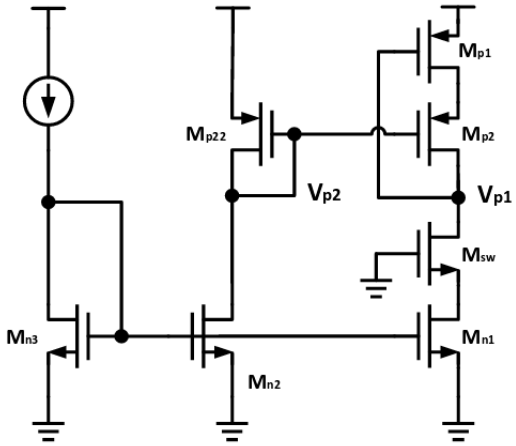


Figure 3.7: Voltage biasing

overdrive voltage and calculated from the desired $\sigma_{\Delta I_D/I_D}$. The size of M_{P22} is determined by choosing the desired V_{p2} needed to ensure enough headroom for M_{p1}. V_{P1} and V_{P2} can be determined by:

$$V_{P1} = V_H - V_{OV,M_{P1}} - V_{TH,M_{P1}} \tag{3.16}$$

$$V_{P2} = V_H - V_{OV,M_{P1}} - V_{OV,M_{P2}} - V_{TH,M_{P2}} \tag{3.17}$$

With large overdrive voltage of M_{P1} to achieve minimal current mismatch, the overdrive voltage of M_{P2} needs to be small, which requires large W of M_{P2} to realize. In addition, the intrinsic gain of M_{P2} needs to be large for better drain-source voltage shielding and this requires large L to realize. The increase in W and L of M_{P2} results in area penalty. After fixing the size of M_{P1}, M_{P2} and M_{P22}, the size of M_{n1}, M_{N2} and M_{N3} can be determined. Due to the fact that the $V_{DS,M_{n1}}$ is different from $V_{DS,M_{n2}}$ and $V_{DS,M_{n3}}$, the width of M_{n2} and M_{n3} will be slightly different from M_{n1}, which in turn results in current mismatch in mirroring. Luckily, the current mismatch in the NMOS is not a big problem as it only introduces gain and offset in the converter.

3.5.2 Current source

Each bit requires a current source. Since the mismatch among current sources greatly affects the linearity of the converter, the gate-source voltage and drain-source voltage of the current branches must be designed to be as close

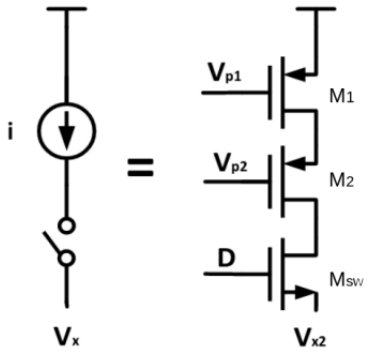


Figure 3.8: Cascode current source

as possible. In order to shield the systematic error due to ΔV_{DS}, a low voltage cascode current source as shown in Fig. 3.8 is chosen as the current source architecture. The intrinsic gain of M_2 determines the strength in resisting the variation in V_x in current mirroring. The variation in drain-source voltage of M_{P1} (Fig. 3.7) sees attenuated variation in V_x; hence, the V_{DS} of M_1 is closer to the V_{DS} of the current mirror M_{P1}, resulting in better current matching. The NMOS below M_2 acts as a switch to turn on or off the current branch. The on-resistance of the NMOS is governed by

$$R_{ON} = \frac{1}{\mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH})} \tag{3.18}$$

Hence, the width of the NMOS needs to be large while keeping the length small so that the on-resistance is small and the voltage drop across the NMOS can be minimized. The size of M_1 and its overdrive voltage V_{OV} play important roles in determining the current mismatch due to random error. As described in (3.12), large W, L and V_{OV} lead to smaller $\sigma_{\Delta I/I}$. The supply voltage V_H of the system is a limiting factor in achieving high V_{OV} due to insufficient headroom to keep all transistors in saturation, which leads to larger device sizing in order to achieve smaller mismatch.

3.5.3 Resistor

There are only two values of resistors used in the R-2R network: R and 2R. A P+ poly resistor without silicide is chosen for the network because it has the highest resistance density with a smaller area. As described previously,

the resistors suffer from mismatch due to geometric and process variation. Hence, the width of the resistor can be increased to reduce resistor mismatch. However, the resistor variation is not a dominant factor of the non-linearity; therefore, it can be kept at minimal width.

3.5.4 Decimal-to-digital code generator

In order to study the static performance of the DAC, the system needs to be tested with all digital code. A decimal-to-digital code generator is written in VerilogA to produce all combinations of the digital code in binary by sweeping the input in decimal from 0 to $(2^N - 1)$.

The overall schematic of the proposed R-2R DAC is shown in Fig. 3.9. This schematic is used to perform simulation in the next chapter.

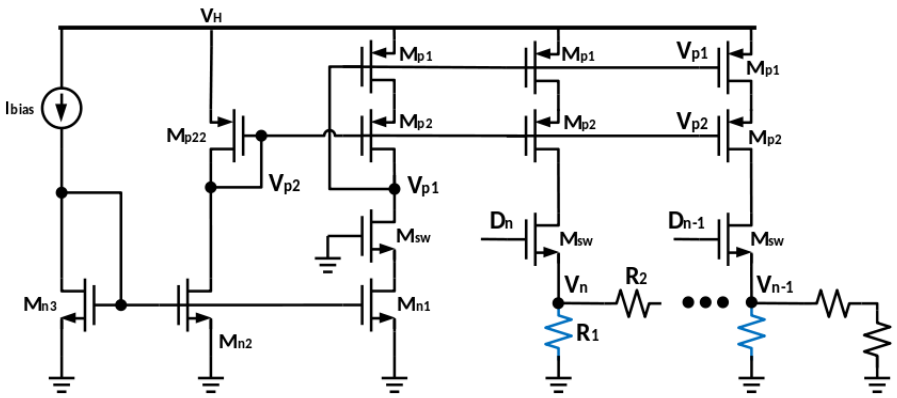


Figure 3.9: Proposed R-2R DAC in transistor level

CHAPTER 4

SIMULATION RESULTS ON R-2R DAC

This chapter presents the simulation result of the ideal DAC using behavioral prototype with specifications listed in Table 3.1. The simulation result of the ideal DAC will then be used as reference to compare with the simulation result of the non-ideal DAC using transistor-level prototype. The non-ideal DAC will cover the simulation result using standard VT PMOS transistor (pch), and 2.5 V high VT PMOS transistor (pch_25), with the aim of achieving DNL $\leq \pm$ 1 LSB.

4.1 Ideal DAC

As described in Section 3.4, the behavior modeling using ideal components gives a perfect output voltage V_{out} transfer curve (Fig. 4.1) with each step of code resulting in 1 LSB increment. The simulation is carried out by sweeping the input voltage V_{dec} of the decimal-to-binary generator (dec2bin) from 0 to 1023 with increment of 1. The output transfer curve should result in 0 DNL and INL as shown in Fig . 4.2. The DNL and INL of the converter are computed using the DNL and INL function in Cadence calculator. Table 4.1 shows the voltages seen at each node in Fig. 3.3 to illustrate the cause of systematic errors in current branches.

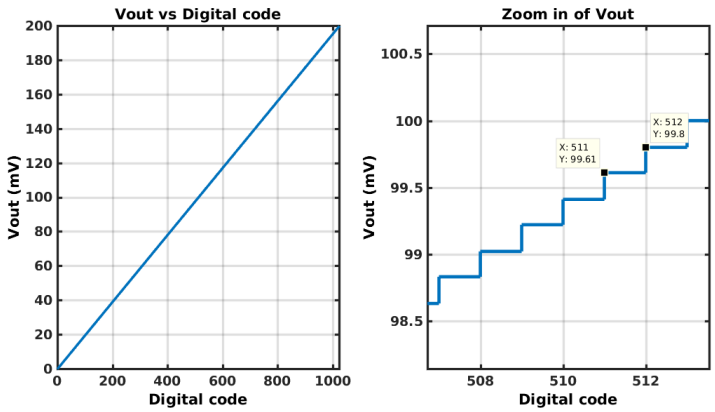


Figure 4.1: Ideal output voltage transfer curve

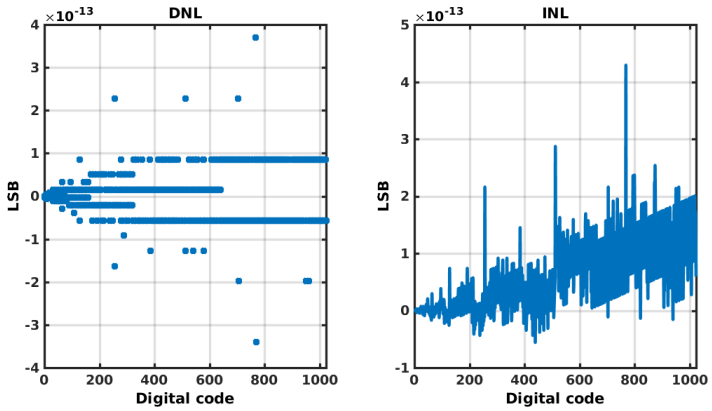


Figure 4.2: DNL and INL of the ideal output voltage

Table 4.1: Node voltages

Decimal code	511	512
Node voltage	(mV)	(mV)
V_{out}	99.805	100.000
V_9	149.707	50.000
V_8	174.463	25.000
V_7	186.450	12.500
V_6	191.663	6.250
V_5	192.706	3.125
V_4	190.103	1.563
V_3	186.450	0.781
V_2	166.276	0.391
V_1	133.138	0.195

4.2 Non-ideal DAC

The non-ideal DAC is simulated in four different cases to study the effect of current mismatch on the performance of the DAC.

4.2.1 Case 1

Before showing the output transfer curve of the non-ideal DAC, the simulation results on voltage biasing and mismatch between two current branches are studied. All the MOSFETs used in the circuit shown in Fig. 3.7 are 1.2 V Standard VT MOS (pch and nch) except for the switch MOSFET (labeled M_{sw}). The sizing for the circuit in Fig.3.7 is set up following Table 4.2 and the simulated operating points are tabulated in Table 4.3. Ignoring the effect of β for simplification, $\sigma_{(\Delta I_D/I_D)_{cal}}$ is computed using (3.12):

$$\sigma_{(\Delta I_D/I_D)_{cal}} = \sqrt{\frac{4(2.7455 \times 10^3)^2}{(6.6 \times 20)0.52^2}} = 0.92m \tag{4.1}$$

After the biasing circuit is set up, the simulation is run on two current branches as shown in Fig. 4.3 with the same sizing as the voltage biasing circuit to study the effect of current mismatch due to systematic and random errors. To study the effect of current mismatch due to systematic error, voltage sources with 0 V and 200 mV are attached to V_n and V_{n-1} respectively in the circuit shown in Fig. 4.3.

Table 4.2: Device sizing

Device	Size (μm/μm)
M_{P1}	6.60/20
M_{P2}	12/0.72
M_{P22}	0.15/1.0
M_{sw}	2/0.28
M_{N1}	0.150/0.40
M_{N2}	0.165/0.40
M_{N3}	0.230/0.40

Table 4.3: Simulated operating points

Parameter	Value	Unit
I_{bias}	5	μ A
V_H	1.20	V
$\sigma_{(\Delta I_D/I_D)_{cal}}$	0.92	m
$(\frac{g_m}{g_{ds}})_{M_{P2}}$	75	
$V_{OV,M_{P1}}$	520	mV
$V_{OV,M_{P2}}$	87	mV
V_{OV,M_n}	215	mV
$V_{drop,SW}$	8	mV
V_{P1}	326	mV
V_{P2}	279	mV

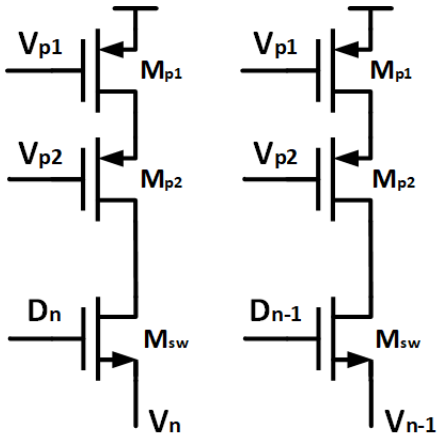


Figure 4.3: Setup for analysis of current mismatch

ΔI and $\Delta I/I$ are the metrics of interest in determining systematic error. ΔI is obtained by subtracting the current I_2 through the voltage source attached at node V_{n-1} with the current I_1 through the voltage source attached at node V_n, while $\Delta I/I$ are computed as

$$\Delta I/I = \frac{I_2 - I_1}{I_1} \tag{4.2}$$

The systematic error calculated using (4.2) from the simulation result is $\Delta I/I = 730\mu$. This value can be reduced if the intrinsic gain $(\frac{g_m}{g_{ds}})_{M_{P2}}$ is higher with the penalty of larger area as described in Chapter 3. The voltage sources are then removed and the nodes are connected to ground to study the effect of current mismatch due to random error. Monte Carlo simulation is performed on the circuit and the result is tabulated in Table 4.4. The simulation result of $\sigma_{\Delta I_D/I_D}$ obtained from Monte Carlo matched the calculated value. A high precision converter (i.e. 10-bits DAC) requires very small $\sigma_{\Delta I/I}$ to achieve DNL $\leq \pm$ 1 LSB. For a lower precision converter, $\sigma_{\Delta I/I}$ can be targeted at a higher value which can be achieved with smaller device sizing.

Table 4.4: Current mismatch due to random errors

MC 200 runs	Mean	Std
$\Delta I/I$	-85.73μ	930μ

After obtaining the current branches and voltage biasing with desired $\sigma_{\Delta I/I}$, the block is tested on a 10-bit DAC to study its performance. Figs. 4.4 and 4.5 show the output transfer curve and the static performance of the

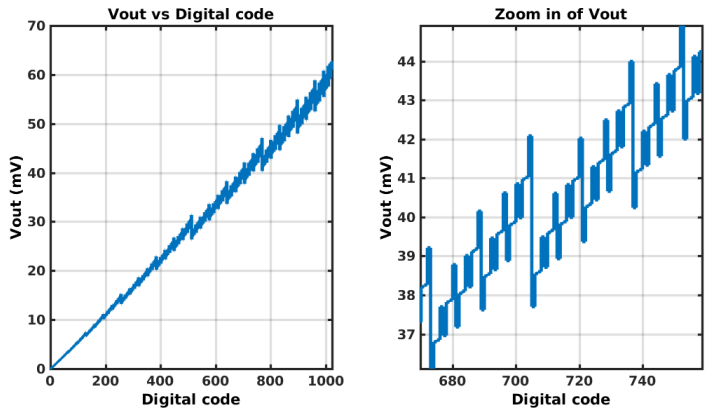


Figure 4.4: Output voltage transfer curve

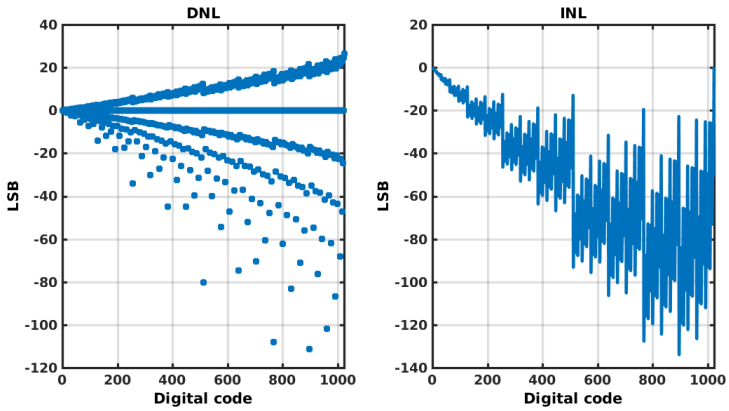


Figure 4.5: Static performance of converter

converter. Unfortunately, the output transfer curve and the static performance are far from expected results due to current leakage in the system. The MOSFETs in 65 nm technology suffer from huge current leakage if the sizing of the device is large. The current through M_{P1} and M_{P22} is no longer maintained at 5 μA but varies when digital code is swept. This variation causes the biasing voltage V_{P1} and V_{P2} (Fig. 4.6) to vary significantly and disturb the biasing on current branches. Current leakage can be minimized for smaller device sizing and higher I_{bias}, but smaller device sizing worsens the current matching. The effect of current matching on device sizing is studied by attaching a voltage-controlled-voltage source (VCVS) on nodes V_{P1} and V_{P2} to prevent the current leakage from affecting the constant voltage biasing so that the static performance of the DAC can be analyzed. Fig. 4.7 shows the output transfer curve and the static performance of the 10-bit DAC due to systematic error only after isolating the current leakage from the

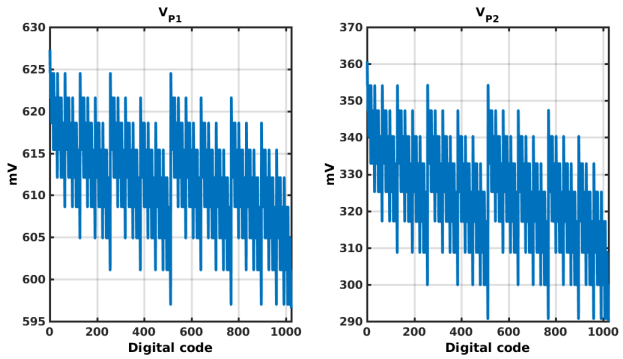


Figure 4.6: Variation on voltage biasing due to current leakage

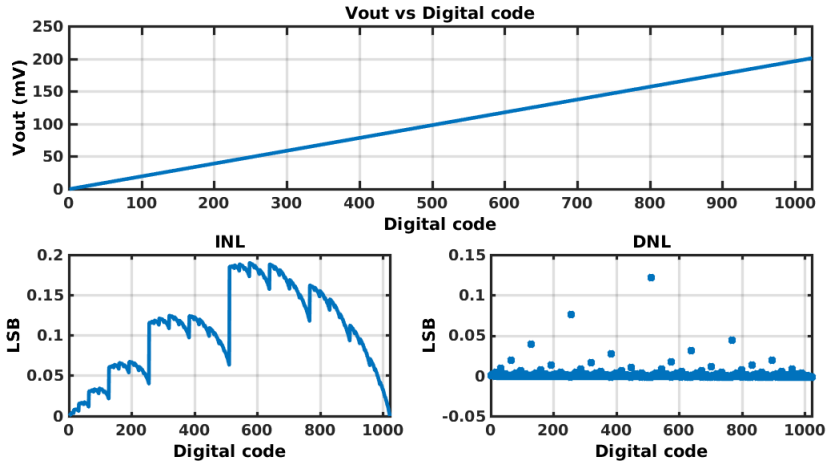


Figure 4.7: Output transfer curve and static performance

system. The DNL is the highest when the decimal code transitions from 511 to 512. This value can be reduced if the intrinsic gain of M_{P2} is increased. The detailed explanation of the spike is illustrated in Table 4.5. As seen from Table 4.5, the currents at each node when decimal code equals 511 are different from each other due to variation in node voltages, which in return causes systematic error in current mirroring. When the current branches are off, there is small leakage current (in femto- or picoampere) flowing through the branches that causes more errors in the transfer curve. The converter is further tested using Monte Carlo simulation to study the effect of random error on its static performance. The Monte Carlo simulation result is reported in Fig. 4.8 and Table 4.6. The experiment is repeated by reducing the W and L of M_{P1} by half to study the impact of the sizing on current mismatch (case 2).

Table 4.5: Current and voltage at each node

Decimal code	511		512	
Node	Current (A)	Voltage (mV)	Current (A)	Voltage (mV)
N_{out}	153.968f	100.389	2.835p	100.610
N_8	5.03339μ	150.584	2.81886p	50.305
N_7	5.03294μ	175.479	2.78685p	25.152
N_6	5.03271μ	187.531	2.72393p	12.576
N_5	5.03262μ	192.771	2.60232p	6.288
N_4	5.03260μ	192.771	2.37514p	3.144
N_3	5.03265μ	191.203	1.97851p	1.572
N_2	5.03279μ	183.612	1.37281p	0.786
N_1	5.03309μ	167.248	660.789f	0.393
N_0	5.03368μ	133.923	5.03395μ	0.197

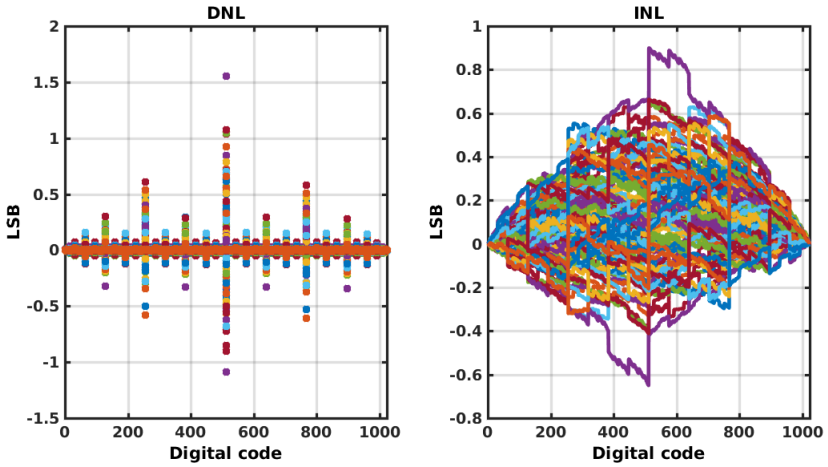


Figure 4.8: Static performance on Monte Carlo

Table 4.6: Summary of INL and DNL from Monte Carlo simulation

MC 200 Runs	Worse case	Mean [LSB]	Std [LSB]
DNL (max/min)	1.550/-1.139	0.358/-0.229	0.266/0.222
INL (max/min)	0.899/-0.650	0.400/-0.145	0.124/0.117

4.2.2 Case 3

To resolve the issue of current leakage in voltage biasing, the standard thin oxide MOSFETs (M_{P1}, M_{P2}, M_{P22}) are replaced with thick oxide MOSFETs (pch_25). Since the thick oxide could handle large supply voltage, V_H is raised to 1.8 V to optimize the design. With higher supply voltage, the overdrive voltage for M_{P1} can be raised to lower its device size in achieving small $\sigma_{\Delta I/I}$

for better current matching. Tables 4.7 and 4.8 show the sizing and operating points of the thick oxide devices. Without the need of VCCS attached to node V_{P1} and V_{P2}, the output transfer curve and the static performance shows trends similar to those in Fig 4.7. The circuit is also tested under Monte Carlo simulation and the results are reported in Fig. 4.9 and Table 4.9. The experiment is repeated with W and L of M_{P1} reduced by half (case 4).

Table 4.7: Device sizing

Device	Size (μm/μm)
M_{P1}	16/24
M_{P2}	10/0.5
M_{P22}	0.4/1.2
M_{sw}	2/0.28
M_{N1}	0.26/2
M_{N2}	0.26/2
M_{N3}	0.26/2

Table 4.8: Simulated operating points

Parameter	Value	Unit
I_{bias}	5	μ A
V_H	1.80	V
$\sigma_{(\Delta I_D/I_D)_{cal}}$	1.4	m
$(\frac{g_m}{g_{ds}})_{M_{P2}}$	110	
$V_{OV,M_{P1}}$	488	mV
$V_{OV,M_{P2}}$	96	mV
V_{OV,M_n}	376	mV
$V_{drop,SW}$	6	mV
V_{P1}	574	mV
V_{P2}	480	mV

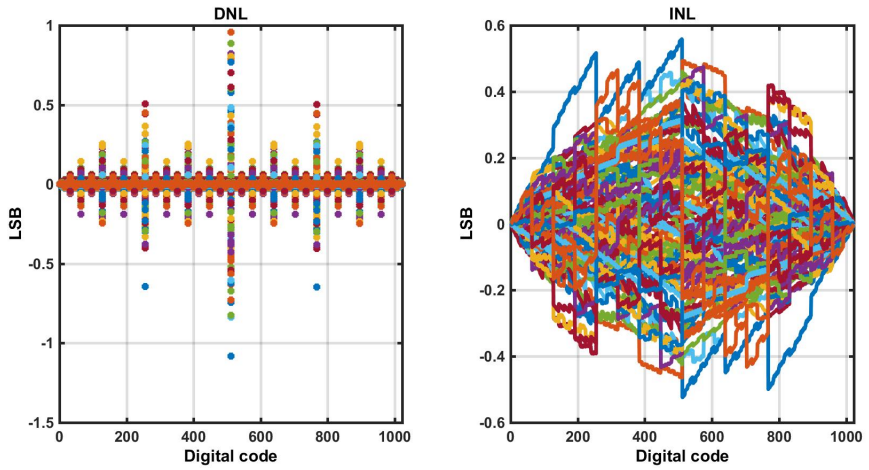


Figure 4.9: Static performance on Monte Carlo

Table 4.9: Summary of INL and DNL from Monte Carlo simulation

MC 200 Runs	Worse case	Mean [LSB]	Std [LSB]
DNL (max/min)	1.125/-1.082	0.269/-0.255	0.243/0.233
INL (max/min)	0.597/-0.564	0.262/-0.229	0.116/0.117

Table 4.10 summarizes the static performance of the converter for four cases:

Case 1 : 1.2 V standard VT PMOS (pch)

Case 2 : Half the length and width of M_{P1} of case 1

Case 3 : 2.5 V standard VT PMOS (pch_25)

Case 4 : Half the length and width of M_{P1} of case 3

Table 4.10: Comparison of the static performance for various experiment setups

Performance		case 1	case 2	case 3	case 4
$\frac{\Delta I}{I}$	Mean	-85.73μ	2.67μ	-	98μ
	Std	930μ	1.86m	1m	1.81m
DNL (max/min) [LSB]	Mean	0.36/-0.23	0.61/-0.36	0.27/-0.26	0.52/-0.50
	Std	0.27/0.22	0.46/0.33	0.24/0.23	0.46/0.43
INL (max/min) [LSB]	Mean	0.40/-0.10	0.66/-0.24	0.26/-0.23	0.48/-0.48
	Std	0.12/0.12	0.22/0.20	0.17/0.12	0.23/0.23
Estimated area (μm^2)		4300	1600	1120	600

From the simulation results in Table 4.10, $\sigma_{\Delta I/I}$ is a major factor in determining the DNL and INL performance of the converter. The smaller the value of $\sigma_{\Delta I/I}$, the better the static performance. However, this improvement comes with the penalty of area. The comparison between the circuits using pch and pch_25 shows significant reduction in area when using thin oxide devices with the condition that the voltage biasing circuit is isolated from the current branches. However, if the area is the main concern in the design, this proposed R-2R DAC will fail to achieve a high precision converter as the simulation result shows that it requires area of more than 600 μm^2 to achieve worst-case DNL, which is less than 1 LSB.

CHAPTER 5

CONCLUSION

In summary, the proposed R2R DAC is simple to construct as it only requires two main components: resistor and current sources. For low precision DAC ($N \leq 6$), the performance of the proposed R2R DAC will be excellent as its DNL can be much less than 1 LSB. However, for higher precision DAC, this proposed architecture sacrifices area to achieve desired performance. The main factor affecting the performance of the proposed R2R DAC is the current mismatch due to random threshold variation. The current mismatch can be further suppressed by increasing overdrive voltage and/or area of the devices. Another result of this work is that the current leakage appears in 65 nm technology and grows significantly when the device size increases; hence, this technology is not suitable to implement any circuitry that requires large sizing. The impact of the current leakage on the system can be reduced by increasing the supply current, which in turn burns more power. Another way of reducing the impact of the current leakage is to isolate the voltage viasing from the current branches, which adds more area to the design.

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